

SRC® High Density MAPstation™ System

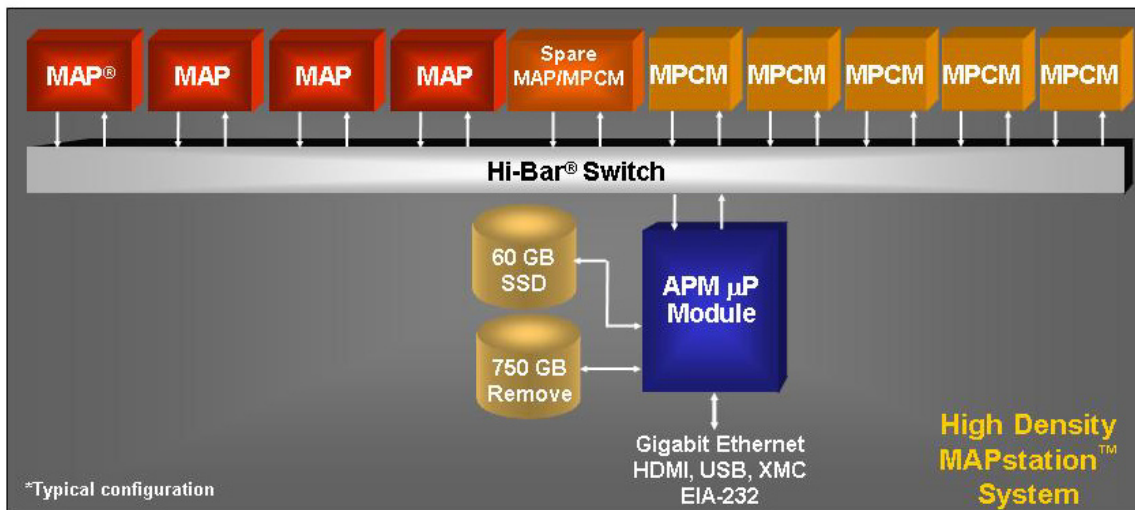
The SRC High Density MAPstation system is a general purpose system targeted at compute intensive problems in a laboratory environment. The 4U high system is designed to fit in standard 19" racks using front to back air flow for cooling. The High Density MAPstation system can be populated with any customer-selected mix of up to 10 modules including MAP® processors, microprocessors and Multi-Ported Common Memory (MPCM) modules.



**Air-Cooled High Density
MAPstation System**

This system is an ideal lower price choice for use as a laboratory development system to duplicate the functionality of an SRC ATLAS™ system having an identical module compliment. All hardware used in the High Density MAPstation system is identical to that used in the rugged ATLAS system, thus eliminating software development risk.

Like all SRC systems, the High Density MAPstation system is programmed using ANSI standard HLLs such as C and Fortran. The SRC Carte™ Programming Environment provides a complete HLL application development, debug, and compilation capability. The Carte Programming Environment tightly integrates all required third party software tools into a single familiar and easy to use environment. Application development for an High Density MAPstation system can also be performed on standard Linux PCs and does not require the use of SRC hardware.



For variations to the standard configuration, contact SRC Computers at sales@srccomputers.com.

SRC® High Density MAPstation™ Specifications

High Density MAPstation Feature	Parameter
Enclosure	
Dimensions	19" W x 27" D x 7" H (48.3 cm W x 68.6 cm D x 17.8 cm H)
Weight with typical 10 module complement	70 pounds (31.8 kg)
Power with typical 10 module complement	500 watts
Input voltage	90-264 VAC, 47-63 Hz (consult SRC Computers for other power options)
External cooling methodology	Air
Removable data disk	Yes
Mounting	Standard rack mount slides
Ambient operating temperature	0°C to +35°C
MAP® Reconfigurable Processor Module	
User Logic	2 Altera EP2S 180 FPGAs
Core clock rate	150 MHz
On Board Memory (OBM) SRAM size	64 Mbytes
On Board Common Memory (OBCM) SDRAM size	2 Gbytes
# simultaneous 64-bit OBM references per clock	16
# simultaneous User Logic DMAs	4 (2 in & 2 out)
Sustained aggregate DMA payload bandwidth	14.4 Gbytes/s
Sustained GPIOX bandwidth	12 Gbytes/s
APM Microprocessor Module	
Microprocessor type	Intel Atom™
Clock rate	1.4 GHz
Total SDRAM memory size	2 Gbytes
Integrated SNAP™ interface bandwidth	3.6 Gbytes/s
I/O available	HDMI, GigE, RS-232, USB, ESATA
Disk	1.8" On-Board
Multi-Ported Common Memory (MPCM)	
SDRAM volume per bank	16 Gbytes
# banks per MPCM module	2
# ports per MPCM	2 in & 2 out
Sustained DMA bandwidth per port	3.6 Gbytes/s
Hi-Bar® Crossbar Switch	
# input ports	16
# output ports	16
Sustained payload bandwidth per port	3.6 Gbytes/s
Aggregate payload bandwidth	57.6 Gbytes/s
Interconnect media to modules	Ribbonized Microcoax