

Wavelet Spectral Dimension Reduction of Hyperspectral Imagery on a Reconfigurable Computer

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Abstract

Hyperspectral imagery, by definition, provides valuable remote sensing observations at hundreds of frequency bands. Conventional image classification (interpretation) methods may not be used without dimension reduction preprocessing. Automatic Wavelet Reduction has been proven to yield better or comparable classification accuracy, while achieving substantial computational savings. However, the large hyperspectral data volumes remain to present a challenge for traditional processing techniques. Reconfigurable Computers (RCs) can leverage the synergism between conventional processors and FPGAs to provide low-level hardware functionality at the same level of programmability as general-purpose computers. In this paper, we investigate the potential of using RCs for on-board, i.e. aboard airborne/spaceborne carriers, preprocessing of hyperspectral imagery by prototyping for the first time the automatic wavelet dimension reduction algorithm. Our investigation exploits the fine and coarse grain parallelism provided by the RCs and has been experimentally verified on one of the state-of-the art reconfigurable platforms, SRC-6E. An order of magnitude speedup over traditional processing techniques has been reported.

1. Introduction

Dimension reduction is the transformation that brings data from a high order dimension to a low order dimension [1]. Dimension reduction has become a significant step for on-board preprocessing of hyperspectral imagery, e.g. image interpretation/classification [2]. In remote sensing, one of the most widely used dimension reduction techniques is the Principal Component Analysis (PCA). PCA, by definition, computes orthogonal projections, which results in time-consuming computations, inefficient use of the memory hierarchy, and finally, large interprocessor communication overhead. For these reasons, the novel Automatic Wavelet Dimension Reduction technique has been recently introduced in [3] and has been proven to yield better or comparable

classification accuracy, while achieving substantial computational savings. However, the large hyperspectral data volumes remain to present a challenge for traditional processing techniques even with the wavelet-based method. Therefore, there is always a pressing need for new efficient and powerful processing capabilities for the implementation of dimension reduction algorithms within the domain of hyperspectral imagery processing.

Reconfigurable Computers (RCs) combine the flexibility of traditional microprocessors with the power of Field Programmable Gate Arrays (FPGAs). These platforms have always been reported to outperform the conventional platforms in terms of throughput and processing power within the domain of encryption, decryption, and image processing applications [4], [5], [6], and [7]. In addition, they are characterized by lower form/wrap factors compared to parallel platforms, and higher flexibility than ASIC solutions. Therefore, RCs are a promising candidate for on-board preprocessing of hyperspectral imagery. The SRC-6E Reconfigurable Computer is one example of this category of hybrid computers [8] and is used here for this purpose.

In this paper, we investigate the potential of using RCs for on-board preprocessing of hyperspectral imagery by prototyping, for the first time, the novel automatic wavelet-based dimension reduction algorithm. This effort is performed by exploiting both the fine-grain and coarse-grain parallelism provided by RCs, seeking optimal speedup gains. The experimental work has been performed on one of the state-of-the art reconfigurable platforms, SRC-6E. An order of magnitude speedup gain has been reported using the P3 version of SRC-6E. These results, although obtained while I/O is still dominating, confirm the efficiency of the proposed solution as well as prove the potential and superiority of the RCs over traditional processing techniques within the domain of hyperspectral imagery.

2. Wavelet-Based Dimension Reduction

2.1. General Description of the Algorithm

The general description of the automatic wavelet dimension reduction algorithm is shown in Fig. 1.

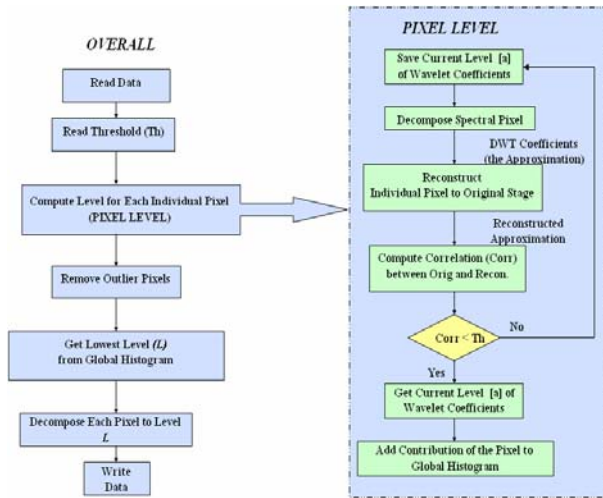


Figure 1. Automatic Wavelet Spectral Dimension Reduction Algorithm

2.2 Automatic Decomposition Level Selection

The correlation function (ρ) between the original spectral signature (x), i.e. the original image, and its reconstructed approximation (y), which results from applying the discrete wavelet transform (DWT) and inverse discrete wavelet transform (IDWT), is defined in equation (1):

$$\rho(x, y) = \frac{\sum_{i=1}^N x_i y_i - \left(\frac{1}{N}\right) \sum_{i=1}^N x_i \sum_{i=1}^N y_i}{\sqrt{\left(\sum_{i=1}^N x_i^2 - \left(\frac{1}{N}\right) \left(\sum_{i=1}^N x_i\right)^2\right) \left(\sum_{i=1}^N y_i^2 - \left(\frac{1}{N}\right) \left(\sum_{i=1}^N y_i\right)^2\right)}} \quad (1)$$

where N represents the original dimension of the hyperspectral image.

Correlation is applied as a quantitative indicator [3], which measures the similarity [9], [10] between the original spectral signature and the reconstructed spectral approximation.

The automatic wavelet spectral reduction algorithm is developed using this correlation measure and a user specified threshold (Th).

In this work, we used the Salinas'98 scene which consists of 217x512 pixels by 192 bands for a total \approx 20MB of radiance data. The Salinas'98 scene was acquired by the Airborne Visible Infrared Imaging Spectrometer (AVIRIS).

3. SRC-6E Reconfigurable Computer

3.1. Hardware Architecture

SRC-6E platform consists of two general-purpose microprocessor boards and one MAP[®] reconfigurable processor board. Each microprocessor board is based on two 1 GHz Pentium 3 microprocessors. The SRC MAP board consists of two MAP reconfigurable processors.

Overall, the SRC-6E system provides a 1:1 microprocessor to FPGA ratio. Microprocessor boards are connected to the MAP board through the SNAP[®] interconnect. SNAP card plugs into the DIMM slot on the microprocessor motherboard [8].

Hardware architecture of the SRC MAP processor is shown in Fig. 2. This processor consists of two programmable User FPGAs, six 4 MB banks of the on-board memory (OBM), and a single Control FPGA. The FPGAs are all Xilinx Virtex II-6000-4.

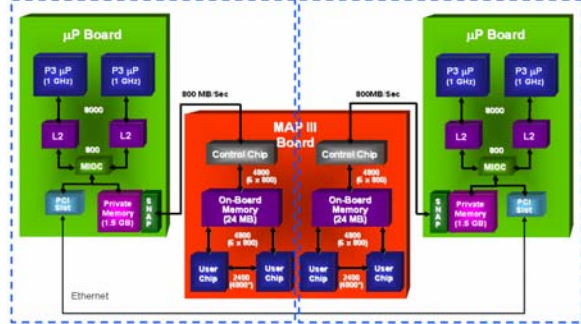


Figure 2. Hardware Architecture of SRC-6E

3.2. Programming Model

The SRC-6E has a similar compilation process as a conventional microprocessor-based computing system, but needs to support additional tasks in order to produce logic for the MAP reconfigurable processor, as shown in Fig. 3. Since users often wish to extend the built-in set of operators, the compiler allows users to integrate their own VHDL/Verilog macros.

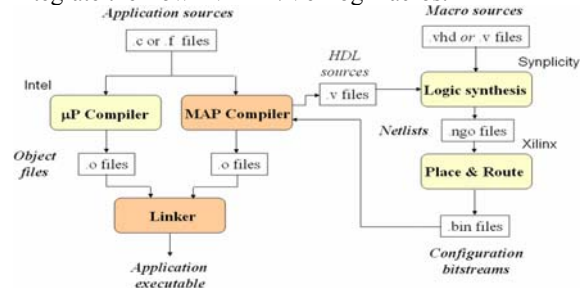


Figure 3. SRC Compilation Process

4. Algorithm Implementation

It is obvious from Fig. 1 that the “PIXEL LEVEL” is the most computational intensive function which represents the bottleneck of the algorithm implementations on traditional platforms. Depending on the separability property of individual pixels, the algorithm lends itself to parallelization, full pipelining, within this specific function. Fig. 4 shows the top hierarchical level of the implementation architecture. The algorithm parallelism has been equally distributed along the pipelined architecture, which, in contrast to the sequential implementations on traditional computers, will expectedly yield significant speedup gains in performance.

A major component of the implementation architecture is the DWT_IDWT module which performs both the Discrete Wavelet Transform (DWT) and the Inverse Discrete Wavelet Transform (IDWT) functions, thus producing the decomposition spectrum, i.e. L1-L5, as well as the reconstruction spectrum, i.e. Y1-Y5, respectively, see Fig. 5. The filtering (L , L') and down/up sampling operations are performed internally with full precision fixed-point signed (two's

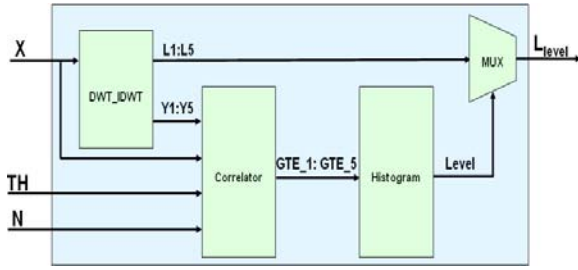


Figure 4. Top Hierarchical Architecture of the Automatic Wavelet Dimension Reduction Algorithm

complement) data types. Truncation was used for quantization and saturated arithmetic was used for overflow handling. The data was externally interfaced into and out from this component under 8-bit precision unsigned data type.

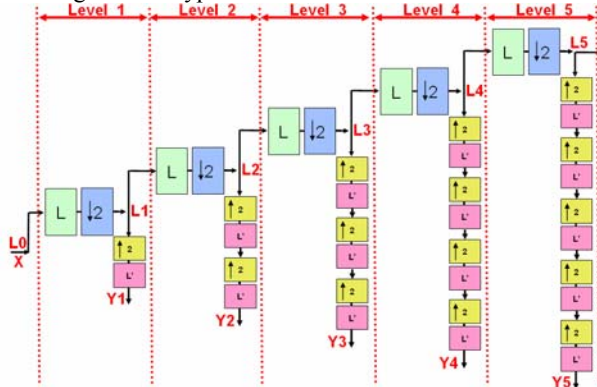


Figure 5. DWT_IDWT Module

The second major component is the Correlator, refer to equation (1). The division and the square-root operations have been avoided when evaluating the correlation function, see Fig. 6. The threshold (TH) has been interpreted with 16-bit precision unsigned data type. The dimension of the hyperspectral image (N) has been interpreted with 8-bit precision unsigned type, thus accommodating for the maximum possible number of hyperspectral bands, typically 220-240 bands. The internal arithmetic operations of the Correlator component have been performed under full-precision fixed-point unsigned data types.

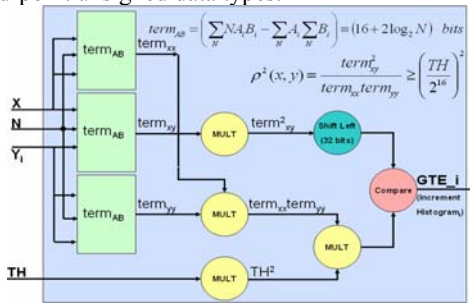


Figure 6. Correlator Module

The built-in multipliers, i.e. MULT18X18, of the FPGA, have been utilized, 81% as shown in Table 1., for implementing both the DWT_IDWT and the Correlator modules.

Table 1. Resource Utilization and Operating Frequency

Slice Utilization (%)		Total 4-Input LUTs Utilization (%)				MULT18X18 (%)	Frequency (MHz)
Flip Flops	Total	Logic	Route-Thru	Shift Registers	Total		
58	65	43.22	0.61	8.20	52.03	81	100

A final component is the Histogram module. This module, as shown in Fig. 7, is implemented with counters which are updated according to the correlation-threshold inequality, i.e. $\rho \geq TH$.

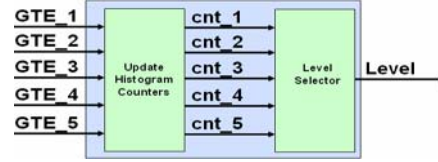


Figure 7. Histogram Module

5. Experimental Work

5.1. Experiment Setups and Measurements Scenarios

The conventional setup on RCs is shown in Fig. 8a. This type of sequential single-transfer is constrained by the size of the OBM bank to/from which the data is to be transferred. Because the hyperspectral datasets are much beyond this constraint, this conventional setup is inconvenient for this specific type of application. We have adopted a multi-transfer approach, as shown in Fig. 8b, in which the data is transferred over multiple streams. The OBM in this approach serves as a buffering mechanism which facilitates streaming the hyperspectral datasets into and out of the RC. The Salinas'98 dataset was processed in 5 streams of 4MB each to fully utilize the OBM banks.

Throughput optimization techniques, such as overlapping, as proposed in [4], and [5] have also been considered for further speedup gains. The application of this technique along with the streaming approach is shown in Fig. 8c.

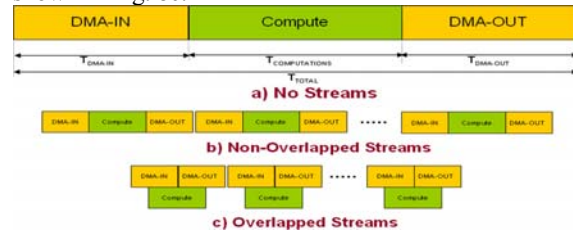


Figure 8. Experiment Setup

Fig. 9 shows the scenarios we have performed for measuring the performance on both the microprocessor and the MAP-processor. We were mainly concerned with the end-to-end execution time, i.e. the total time necessary to manipulate the hyperspectral streams (nstreams).

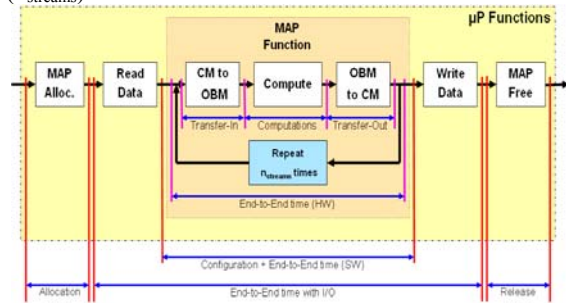


Figure 9. Measurements Scenario

5.2. Experimental Results

Fig. 10 shows the timing results obtained from a 1.8GHz Intel Xeon processor and from SRC-6E. Both the no-overlapping and overlapping approaches have been included in Fig. 10.

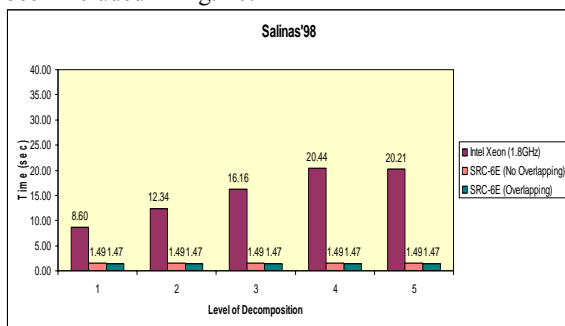


Figure 10. Execution Times

The superiority of RCs over traditional platforms for hyperspectral imagery is demonstrated through the speedup plots shown in Fig. 11.

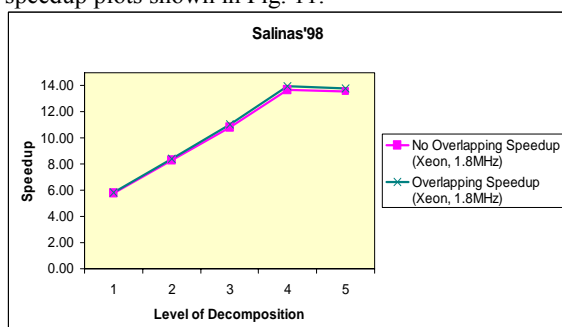


Figure 11. Speedup Results

It is crucial to note in Fig. 10 that, because of the sequential manner by which the algorithm executes on traditional microprocessors, the execution time is proportional to the number of decomposition levels. In contrast to this, the corresponding time on SRC-6E is constant due to the fact that the algorithm has been fully pipelined.

It is also worthy to note that, as was theoretically expected and as shown in both Figs. 10 and 11, the overlapping approach gained insignificant speedup over the non-overlapping approach. This is because the overlapping technique only hides the computations equivalence of the I/O time, 0.4171 ms/stream, which is much less than the total I/O time, 23.8861 ms/stream. This also reflects the fact that the algorithm has been optimally parallelized to the extent that any further optimizations add insignificant gain in performance due to I/O bounds.

6. Conclusions

In this paper, we investigated the potential of using RCs for on-board, i.e. aboard airborne/spaceborne carriers, preprocessing of hyperspectral imagery by implementing for the first time the novel automatic wavelet-based dimension reduction algorithm. The fine and coarse grain parallelism provided by the RCs have also been exploited seeking speedup gains. The experimental verification has been performed on one of

the state-of-the art reconfigurable platforms, SRC-6E. The algorithm has been optimally parallelized and an order of magnitude speedup gain has been reported using the P3 version of SRC-6E. These speedup figures confirm the efficiency of the proposed solution as well as prove the potential and superiority of the RCs over traditional processing techniques within the domain of hyperspectral imagery.

Depending on the separability property of pixels, the wavelet-based dimension reduction technique lends itself very well to superscalable implementations on multiple FPGAs which, expectedly, can improve the performance resulting in higher speedup gains. Furthermore, speedup can be increased by improving the platform I/O constraints, and we expect a significant improvement, almost the double, in speedup when using the P4 version of SRC machine.

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